WHAT IS CLAIMED IS:

1. An array of magnetoresistive random access memory (MRAM) cells disposed on a substrate at intersections of global bit and word lines, comprising:

a plurality of local bit lines, each local bit line electrically coupled to at least one MRAM cell;

a plurality of switches, each switch selectively connecting a global bit line to at least one local bit line; and

a plurality of select lines, each select line having a first terminal coupled to a control input of one of the switches and a second terminal coupled to a controller of read and write operations of an MRAM device comprising at least one said array.

2. The array of claim 1 wherein, during a read operation, the switches connect the global bit line to the local bit line coupled to the selected MRAM cell.

3. The array of claim 1 wherein, during a read operation, the switches disconnect the global bit line from the local bit lines other than the local bit line coupled to the selected MRAM cell.

4. The array of claim 1 wherein, during a write operation, the switches disconnect the global bit line from the local bit lines coupled to the non-selected MRAM cells.

5. The array of claim 1 wherein the switch comprises a field effect transistor.

6. The array of claim 1 wherein each MRAM cell comprises a magnetic tunnel junction having a free magnetic layer and a reference magnetic layer where one of the layers is coupled to the local bit line and the other layer is coupled to the global word line.

7. The array of claim 1 wherein, at the intersections, the global word lines are disposed closer to the substrate than the global and local bit lines.

8. The array of claim 1 wherein, at the intersections, the global and local bit lines

are disposed closer to the substrate than the global word lines.

9. The array of claim 1 wherein the coupled global and local bit lines run parallel one another.

10. The array of claim 1 wherein the coupled global and local bit lines run one above another.

11. The array of claim 1 wherein the coupled global and local bit lines are separated by a dielectric layer disposed between the lines.

12. The array of claim 1 comprising stacked local bit lines, wherein:

the stacked local bit lines are electrically coupled to each other and to the switch selectively connecting the lines to the global bit line;

one stacked bit line is magnetically coupled to the global bit line; and

the remaining stacked local bit lines are each magnetically coupled to a separate global bit line of the MRAM device.

13. A method of fabricating a magnetoresistive random access memory (MRAM) device on a substrate, comprising:

forming at least one array of MRAM cells comprising:

a plurality of local bit lines, each local bit line electrically coupled to at least one MRAM cell;

a plurality of switches, each switch connecting a global bit line to at least one local bit line or disconnecting the global bit line from the at least one local bit line; and

a plurality of select lines, each select line having a first terminal coupled to a control input of one of the switches; and

coupling second terminals of the select lines to a controller of read and write operations of the MRAM device.

14. The method of claim 13 wherein, during a read operation, the switches connect the global bit line to the local bit line coupled to the selected MRAM cell.

15. The method of claim 13 wherein, during a read operation, the switches disconnect the global bit line from the local bit lines other than the local bit line coupled to the selected MRAM cell.

16. The method of claim 13 wherein, during a write operation, the switches disconnect the global bit line from the local bit lines coupled to the non-selected MRAM cells.

17. The method of claim 13 wherein the switch comprises a field effect transistor.

18. The method of claim 13 wherein each MRAM cell comprises a magnetic tunnel junction having a free magnetic layer and a reference magnetic layer where one of the layers is coupled to the local bit line and the other layer is coupled to the global word line.

19. The method of claim 13 wherein, at the intersections, the global word lines are disposed closer to the substrate than the global and local bit lines.

20. The method of claim 13 wherein, at the intersections, the global and local bit lines are disposed closer to the substrate than the global word lines.

21. The method of claim 13 wherein the coupled global and local bit lines run parallel one another.

22. The method of claim 13 wherein the coupled global and local bit lines run one above another.

23. The method of claim 13 wherein the coupled global and local bit lines are separated by a dielectric layer disposed between the lines.

24. The method of claim 13 comprising stacked local bit lines, wherein:

the stacked local bit lines are electrically coupled to each other and to the switch selectively connecting the lines to the global bit line;

one stacked bit line is magnetically coupled to the global bit line; and

the remaining stacked local bit lines are each magnetically coupled to a separate global bit line of the MRAM device.

25. A magnetoresistive random access memory (MRAM) device, comprising at least one array of MRAM cells formed on a substrate, the array comprising:

a plurality of local bit lines, each local bit line electrically coupled to at least one MRAM cell;

a plurality of switches, each switch connecting a global bit line to at least one local bit line or disconnecting the global bit line from the at least one bit local line; and

a plurality of select lines, each select line having a first terminal coupled to a control input of one of the switches; and

a controller of read and write operations coupled to second terminals of the select lines.

26. The MRAM device of claim 25 wherein, during a read operation, the switches connect the global bit line to the local bit line coupled to the selected MRAM cell.

27. The MRAM device of claim 25 wherein, during a read operation, the switches disconnect the global bit line from the local bit lines other than the local bit line coupled to the selected MRAM cell.

28. The MRAM device of claim 25 wherein, during a write operation, the switches disconnect the global bit line from the local bit lines coupled to the non-selected MRAM cells.

29. The MRAM device of claim 25 wherein the switch comprises a field effect transistor.

30. The MRAM device of claim 25 comprising stacked local bit lines, wherein:

the stacked local bit lines are electrically coupled to each other and to the switch selectively connecting the lines to the global bit line;

one stacked bit line is magnetically coupled to the global bit line; and

the remaining stacked local bit lines are each magnetically coupled to a separate global bit line of the MRAM device.

31. A method of increasing a signal-to-noise ratio of a magnetoresistive random access memory (MRAM) device during read and write operations, comprising:

segmenting a global bit line using a plurality of local bit lines, a plurality of switches, and a plurality of select lines, each select line having a first terminal coupled to a control input of one of the switches, wherein each local bit line is coupled to at least one MRAM cell, each switch connects a global bit line to at least one local bit line or disconnects the global bit line from the at least one bit local line; and

setting the switches using a controller of the read and write operations coupled to second terminals of the select lines.

32. The method of claim 31 wherein, during a read operation, the switches connect the global bit line to the local bit line coupled to the selected MRAM cell.

33. The method of claim 31 wherein, during a read operation, the switches disconnect the global bit line from the local bit lines other than the local bit line coupled to the selected MRAM cell.

34. The method of claim 31 wherein, during a write operation, the switches disconnect the global bit line from the local bit lines coupled to the non-selected MRAM cells.

35. The method of claim 31 wherein the switch comprises a field effect transistor.

36. The method of claim 31 comprising stacked local bit lines, wherein:

the stacked local bit lines are electrically coupled to each other and to the switch selectively connecting the lines to the global bit line;

one stacked bit line is magnetically coupled to the global bit line; and

the remaining stacked local bit lines are each magnetically coupled to a separate global bit line of the MRAM device.

37. A magnetoresistive random access memory (MRAM) device, comprising:

(a) a global bit line;

(b) a plurality of cell groups, each cell group comprising at least one MRAM cell; and

(c) a switch for each cell group configured to selectively connect and disconnect the respective cell group from the global bit line.

38. The MRAM device of claim 37 wherein at least one cell group comprises at least one MRAM cell connected by a local bit line, and wherein the local bit line is connected to a terminal of the respective switch.

39. The MRAM device of claim 37 wherein, during a read operation, the switches disconnect the global bit line from the local bit lines other than the local bit line coupled to the selected MRAM cell.

40. The MRAM device of claim 37 wherein, during a write operation, the switches disconnect the global bit line from the local bit lines coupled to the non-selected MRAM cells.

41. The MRAM device of claim 37 wherein the switch comprises a field effect transistor.

42. The MRAM device of claim 37 wherein each MRAM cell comprises a magnetic tunnel junction having a free magnetic layer and a reference magnetic layer where one of the layers is coupled to the local bit line and the other layer is coupled to the global word line.

43. The MRAM device of claim 37 wherein, at the intersections, the global word lines are disposed closer to the substrate than the global and local bit lines.

44. The MRAM device of claim 37 wherein, at the intersections, the global and local bit lines are disposed closer to the substrate than the global word lines.

45. The MRAM device of claim 37 wherein the coupled global and local bit lines run parallel one another.

46. The MRAM device of claim 37 wherein the coupled global and local bit lines run one above another.

47. The MRAM device of claim 37 wherein the coupled global and local bit lines are separated by a dielectric layer disposed between the lines.

48. A method of performing read and write operations in a magnetoresistive random access memory (MRAM) device, comprising:

segmenting a global bit line using a plurality of local bit lines, a plurality of switches, and a plurality of select lines, each select line having a first terminal coupled to a control input of one of the switches, wherein each local bit line is coupled to at least one MRAM cell, each switch connects a global bit line to at least one local bit line or disconnects the global bit line from the at least one bit local line;

setting, during a read operation, the switches to connect the local bit line coupled to the selected MRAM cell and to disconnect the global bit line from the local bit lines other than that local bit line; and

setting, during a write operation, the switches to disconnect the global bit line from the local bit lines coupled to the non-selected MRAM cells.

49. The method of claim 47 wherein the switches are controlled using a controller of the read and write operations coupled to second terminals of the select lines.